

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:
a plurality of memory cells arranged in rows and columns,
said plurality of memory cells being divided into a plurality of
storage units each formed of the two memory cells bearing complementary
5 data;

a plurality of bit lines forming pairs each including the two bit lines
and arranged corresponding to the columns of said memory cells,
respectively;

10 a plurality of word lines arranged corresponding to the rows of said
memory cells, respectively, and extending in a direction crossing said
plurality of bit lines; and

a plurality of cell plates provided corresponding to said storage units,
respectively, and each isolated at least electrically from the others, wherein
each of said plurality of memory cells includes:

15 a select transistor connected between the corresponding bit line and
a storage node, and being turned on or off in accordance with a voltage on
the corresponding word line, and

a capacitor connected between said storage node and the
corresponding cell plate.

2. The semiconductor memory device according to claim 1, wherein
gates of the select transistors in said two memory cells forming the
same storage unit are connected to the word lines different from each other,
respectively.

3. The semiconductor memory device according to claim 2, wherein
each of said plurality of memory cells further includes an active
region extending in an extending direction of the corresponding bit line and
defining a formation region of said select transistor,

5 said active region extends continuously through a portion between
the two memory cells neighboring to each other in the extending direction

of the corresponding bit line, and

said semiconductor memory device further comprises:

10 a bit line contact provided for each of sets each including the
neighboring two memory cells, and electrically connecting the
corresponding active region to the corresponding bit line.

4. The semiconductor memory device according to claim 1, wherein
gates of the select transistors in said two memory cells forming the
same storage unit are connected to the same word line.

5. The semiconductor memory device according to claim 1, wherein
gates of the select transistors in said two memory cells forming the
same storage unit are connected to the same word line,

5 each of said plurality of memory cells further includes an active
region extending in a direction intermediate between an extending
direction of the corresponding word line and an extending direction of the
corresponding bit line, and defining a formation region of said select
transistor,

said semiconductor memory device further comprises:

10 a plurality of bit line contacts connecting the active regions of said
plurality of memory cells to the corresponding bit lines, respectively,

said plurality of bit line contacts are aligned in the extending
direction of said plurality of word lines, and are provided corresponding to
said bit lines, respectively,

15 the two word lines are arranged between said bit line contacts
neighboring to each other in the extending direction of said plurality of bit
lines,

said active regions continuously extend through a portion between
portions each including the two memory cells and neighboring to each other
20 in the extending direction of said active region, and

said bit line contact is shared by the neighboring two memory cells.

6. The semiconductor memory device according to claim 5, further

comprising:

5 a plurality of dummy word lines each arranged in a region between said storage nodes of the memory cells which correspond to the different bit line contacts and neighbor to each other in the extending direction of said plurality of bit lines, respectively, and extending in the same direction as said plurality of word lines.

7. The semiconductor memory device according to claim 6, wherein each of said plurality of dummy word lines carries a voltage at a predetermined level, and
5 said active region continuously extends through a region under each of said dummy word lines.

8. The semiconductor memory device according to claim 7, wherein each of said plurality of dummy word lines carries a voltage at a predetermined level, and
5 said active regions substantially extend continuously in the same direction such that said active regions in the memory cells arranged in the neighboring columns, respectively, and belonging to the neighboring rows, respectively, continue to each other.

9. The semiconductor memory device according to claim 7, wherein each of said plurality of dummy word lines carries a voltage at a predetermined level, and
5 said active regions are continuously formed to be symmetric with respect to each of said dummy word lines.

10. The semiconductor memory device according to claim 6, wherein each of said plurality of dummy word lines carries a voltage at a predetermined level.

11. The semiconductor memory device according to claim 6, wherein an interval between said word line and said dummy word line is

substantially equal to an interval between said word lines.

12. A semiconductor memory device comprising:
a plurality of memory cells arranged in rows and columns,
said plurality of memory cells being divided into a plurality of
storage units each formed of the two memory cells bearing complementary
5 data;
a plurality of bit lines forming pairs each including the two bit lines
and arranged corresponding to the columns of said memory cells,
respectively;
a plurality of word lines arranged corresponding to the rows of said
10 memory cells, respectively, and extending in a direction crossing said
plurality of bit lines; and
a plurality of cell plates provided corresponding to predetermined
sections of said plurality of storage units, respectively, and each isolated at
least electrically from the others, wherein
15 each of said plurality of memory cells includes:
a select transistor connected between the corresponding bit line and
a storage node, and being turned on or off in accordance with a voltage on
the corresponding word line, and
a capacitor connected between said storage node and the
20 corresponding cell plate.

13. A semiconductor memory device comprising:
a plurality of memory cells arranged in rows and columns,
said plurality of memory cells being divided into a plurality of
storage units each formed of the two memory cells bearing complementary
5 data;
a plurality of bit lines forming pairs each including the two bit lines
and arranged corresponding to the columns of said memory cells,
respectively;
a plurality of word lines arranged corresponding to the rows of said
10 memory cells, respectively, and extending in a direction crossing said

plurality of bit lines; and
a plurality of cell plates provided corresponding to said storage units,
respectively, and each isolated at least electrically from the others, wherein
one of said two memory cells forming each of said storage units
15 includes:
a select transistor connected between one of said paired two bit lines
and a storage node, and being turned on or off in accordance with a voltage
on the corresponding word line, and
a capacitor connected between said storage node and the
20 corresponding cell plate; and
the other of said two memory cells forming said storage unit
includes:
a select transistor connected between the other of said paired two bit
lines and said cell plate without interposing a capacitor, and being turned
25 on or off in accordance with the voltage on the corresponding word line.